PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10043458	01/09/2002	716		2825	

**APPLICANTS: Teng Chin-Chi; Dai Wei-Jin;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed ☐ yes ☐ no 35 USC 119 conditions met ☐ yes ☐ no Verified and Acknowledged Examiners's intials			ATTORNEY DOCKET NO SILI 2282

TITLE : Clock tree synthesis for a hierarchically partitioned IC layout

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid	Primary Examiner	Sheets Drwg. / Figs.Drwg. / Print Fig.	Application Examiner
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